

- ★ Super Low Gate Charge
- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

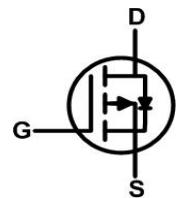
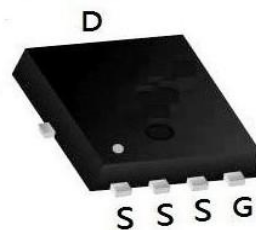
**Product Summary**

BVDSS	RDS(on)	ID
-40V	4.3mΩ	-80 A

**Description**

The XXW80P04F is the high cell density trenched P-ch MOSFETs, which provide excellent RDS(on) and gate charge for most of the synchronous buck converter applications.

The XXW80P04F meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

**PRPAK5X6 Pin Configuration**

**Absolute Maximum Ratings**

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	-40	V
$V_{GS}$	Gate-Source Voltage	±20	V
$I_D@T_C=25^{\circ}C$	Continuous Drain Current, $V_{GS} @ -10V^{1,6}$	-80	A
$I_D@T_C=100^{\circ}C$	Continuous Drain Current, $V_{GS} @ -10V^{1,6}$	-56	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	-320	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	576	mJ
$I_{AS}$	Avalanche Current	-56	A
$P_D@T_C=25^{\circ}C$	Total Power Dissipation <sup>4</sup>	58	W
$T_{STG}$	Storage Temperature Range	-55 to 175	°C
$T_J$	Operating Junction Temperature Range	-55 to 175	°C

**Thermal Data**

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient <sup>1</sup> ( $t \leq 10S$ )	---	20	°C/W
	Thermal Resistance Junction-ambient <sup>1</sup> (Steady State)	---	50	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-case <sup>1</sup>	---	1.6	°C/W

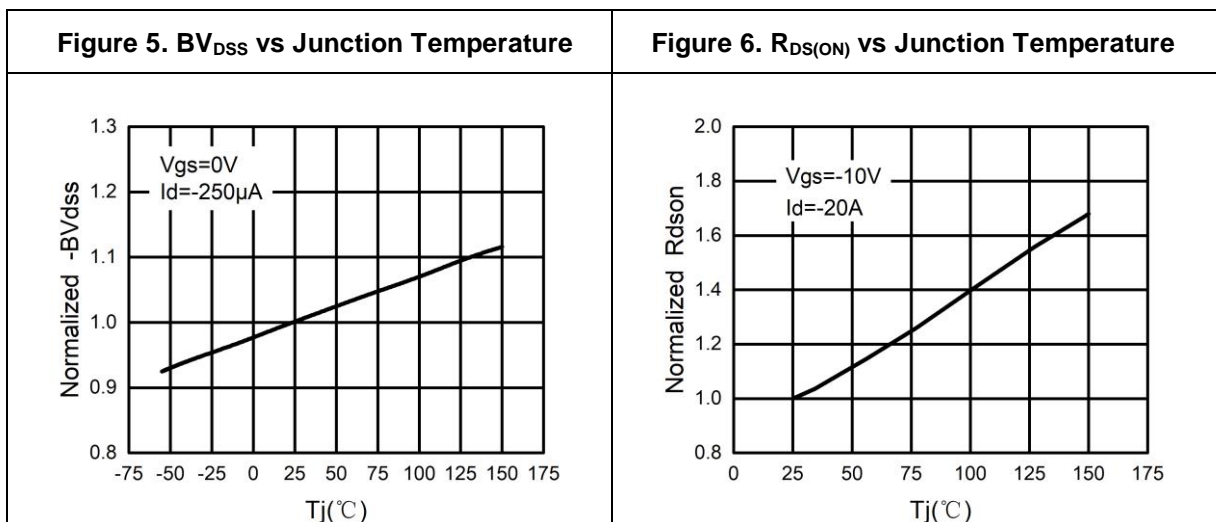
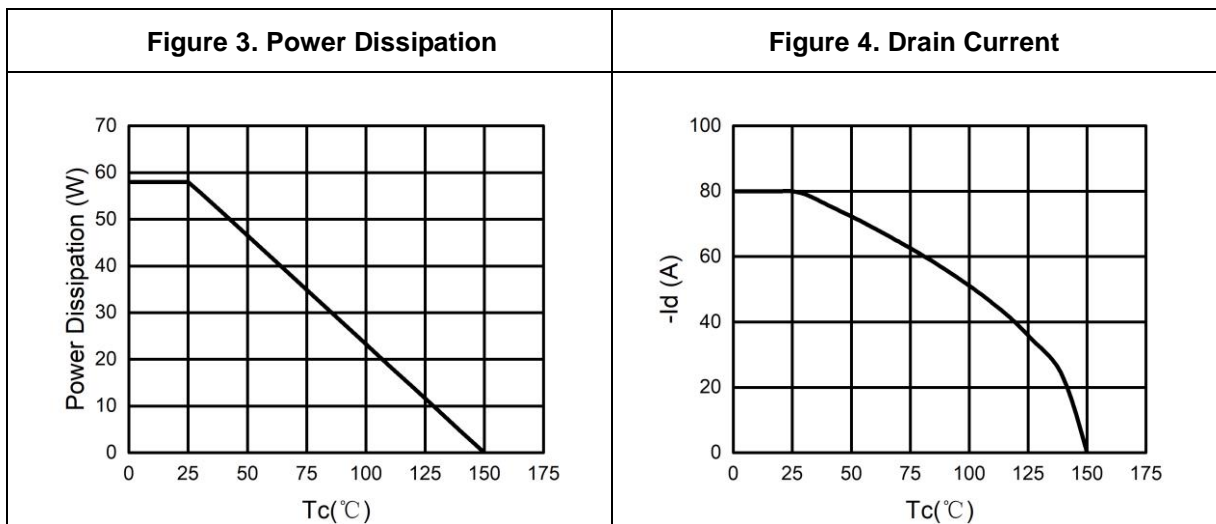
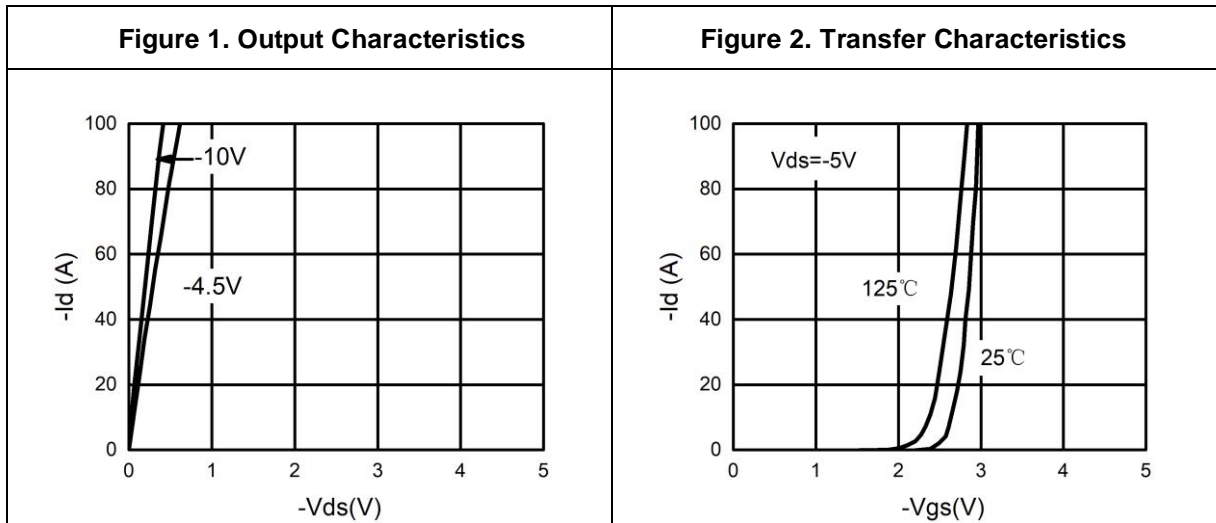
**Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>On/Off States</b>						
B <sub>VDS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V I <sub>D</sub> =-250μA	-40			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =-40V, V <sub>GS</sub> =0V			-1	μA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V			±100	nA
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250μA	-1	-1.7	-2.5	V
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =-5V, I <sub>D</sub> =-20A		63		S
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =-10V, I <sub>D</sub> =-20A		4.3	5.3	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-20A		5.9	7.6	mΩ
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V, f=1.0MHz		6638		pF
C <sub>oss</sub>	Output Capacitance			545		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			345		pF
R <sub>g</sub>	Gate resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1.0MHz		2.2		Ω
<b>Switching Parameters</b>						
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-20V, R <sub>L</sub> =1Ω, R <sub>GEN</sub> =3Ω		16		nS
t <sub>r</sub>	Turn-on Rise Time			17		nS
t <sub>d(off)</sub>	Turn-Off Delay Time			68		nS
t <sub>f</sub>	Turn-Off Fall Time			31		nS
Q <sub>g</sub>	Total Gate Charge	V <sub>GS</sub> =-10V, V <sub>DS</sub> =-20V, I <sub>D</sub> =-20A		118		nC
Q <sub>gs</sub>	Gate-Source Charge			13		nC
Q <sub>gd</sub>	Gate-Drain Charge			22		nC
<b>Source-Drain Diode Characteristics</b>						
I <sub>SD</sub>	Source-Drain Current (Body Diode)				-80	A
V <sub>SD</sub>	Forward on Voltage (Note 3)	V <sub>GS</sub> =0V, I <sub>S</sub> =-20A			-1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> =-20A, di/dt=500A/μs		24		ns
Q <sub>rr</sub>	Reverse Recovery Charge	I <sub>F</sub> =-20A, di/dt=500A/μs		140		nC

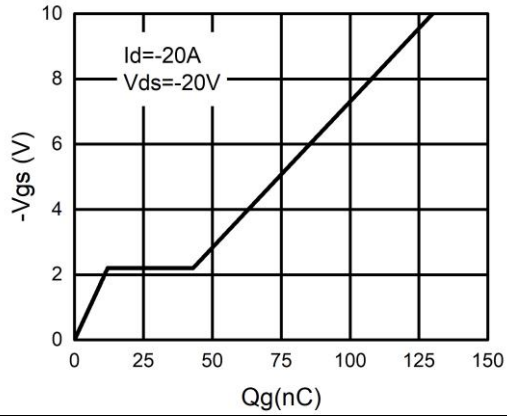
Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature.

Notes 2.E<sub>AS</sub> condition: T<sub>J</sub>=25 °C, V<sub>DD</sub>=15V, V<sub>G</sub>=-10V, R<sub>g</sub>=25Ω, L=0.5mH.

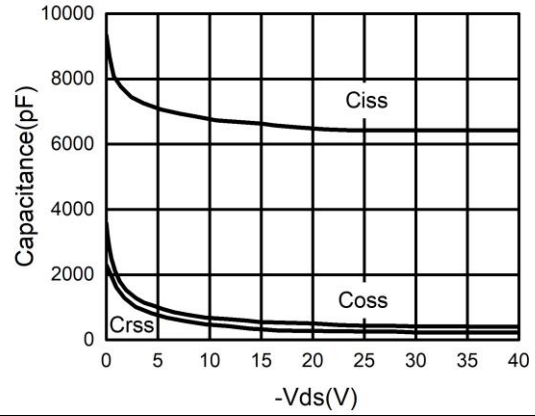
Notes 3.Repetitive Rating: Pulse width limited by maximum junction temperature.

**Typical Electrical And Thermal Characteristics (Curves)**


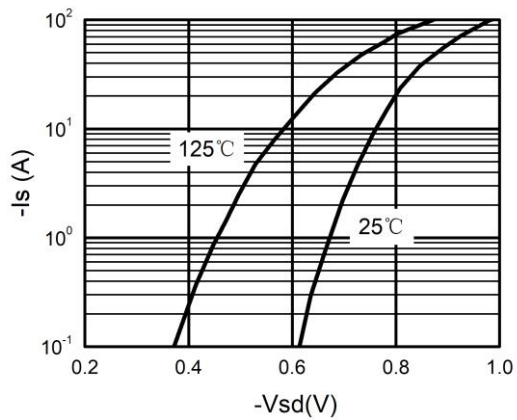
**Figure 7. Gate Charge Waveforms**



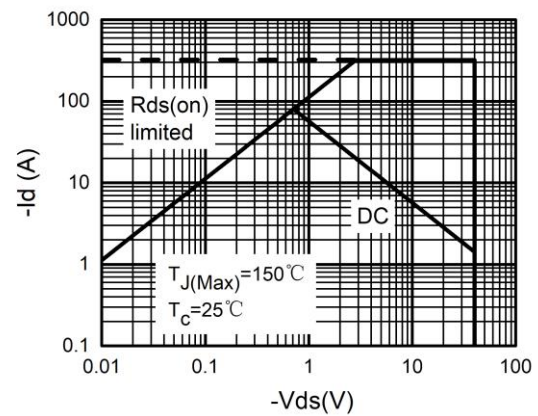
**Figure 8. Capacitance**



**Figure 9. Body-Diode Characteristics**

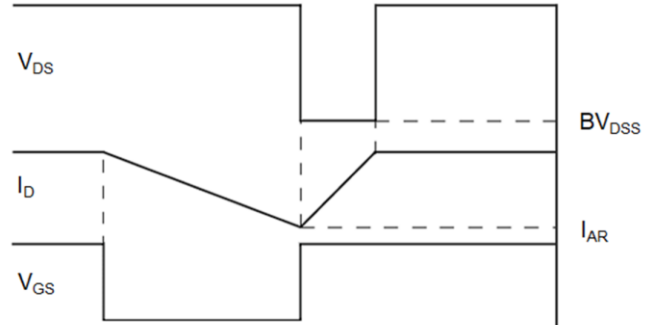
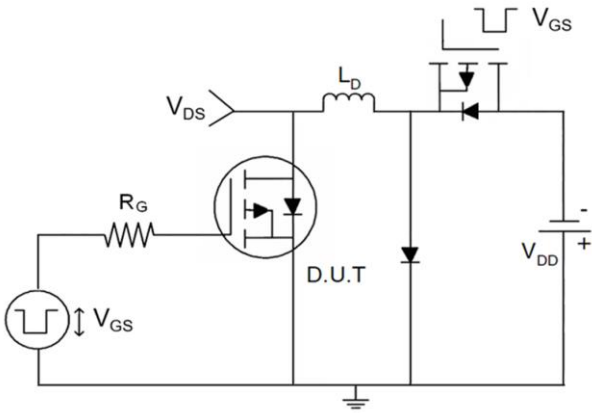


**Figure 10. Maximum Safe Operating Area**

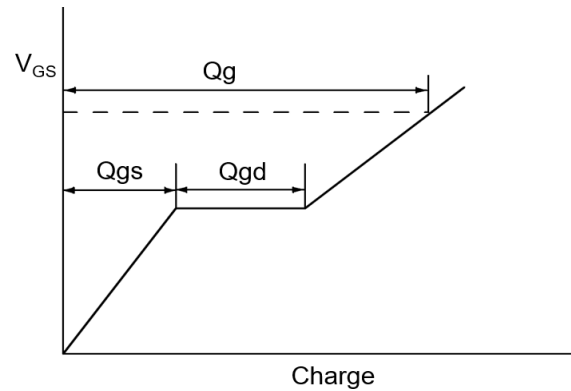
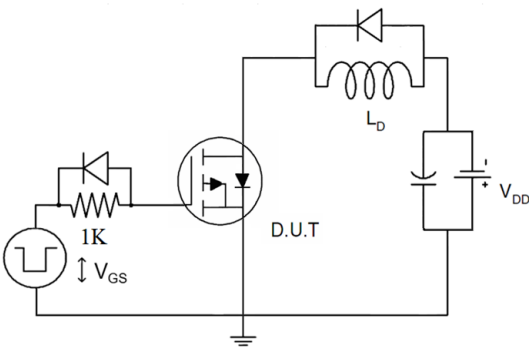


### Test Circuit

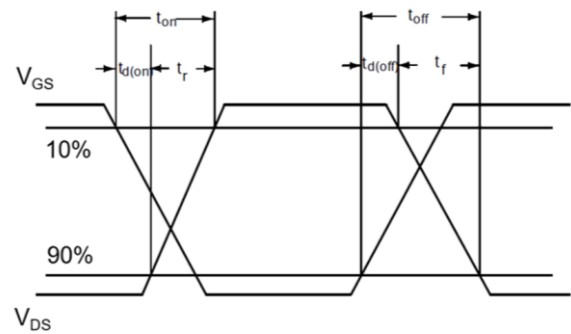
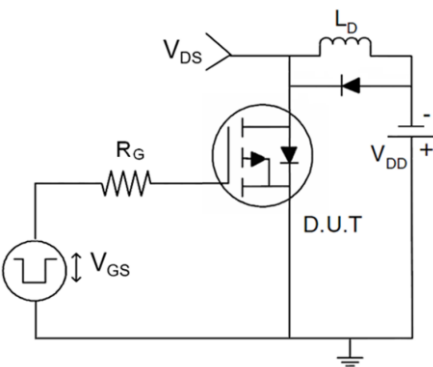
#### 1) $E_{AS}$ Test Circuits

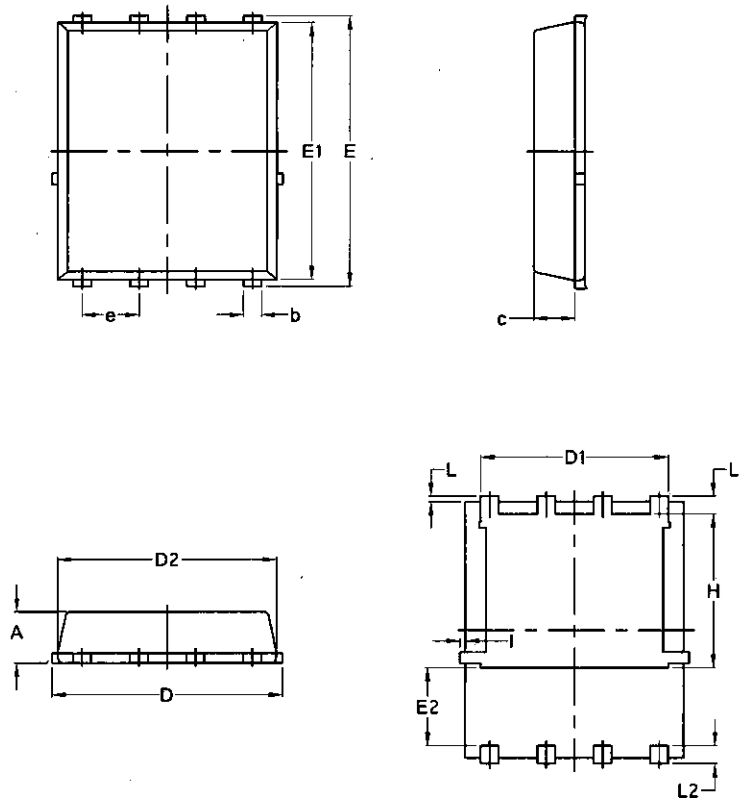


#### 2) Gate Charge Test Circuit



#### 3) Switch Time Test Circuit



**Package Mechanical Data-DFN5\*6-8L-JQ Single**


Symbol	Common			
	mm		Inch	
	Min	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070