

**Features**

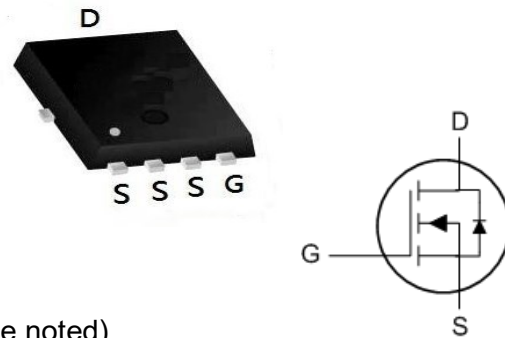
- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low  $R_{DS(ON)}$


**Product Summary**

BVDSS	RDSON	ID
40V	1.1mΩ	225A

**Applications**

- DC-DC Converters
- Power management functions
- Synchronous-rectification applications

**PRPAK5X6 Pin Configuration**

**■ Absolute Maximum Ratings ( $T_A=25^{\circ}\text{C}$  unless otherwise noted)**

Parameter	Symbol	Limit	Unit
Drain-source Voltage	$V_{DS}$	40	V
Gate-source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current (Silicon limited)	$I_D$	225	A
Drain Current <sup>A</sup>	$I_D$	$T_C=25^{\circ}\text{C}$	130
		$T_C=100^{\circ}\text{C}$	82
Pulsed Drain Current <sup>B</sup>	$I_{DM}$	390	A
Avalanche energy <sup>C</sup>	$E_{AS}$	450	mJ
Total Power Dissipation <sup>D</sup>	$P_D$	114	W
Thermal Resistance Junction-to-Case	$R_{\theta JC}$	1.1	°C/W
Thermal Resistance Junction-to-Ambient <sup>E</sup>	$R_{\theta JA}$	20	
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55~+150	°C

**N-Ch 40V Fast Switching MOSFETs**
**■ Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise noted)**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> =250μA	40	48		V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =40V, V <sub>GS</sub> =0V			1	μA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			±100	nA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> =250μA	1.2	1.8	2.5	V
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> =20A		1.1	1.4	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> =20A		1.7	2.3	
Gate Resistance	R <sub>g</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> Open, f=1MHZ		2.7		Ω
Maximum Body-Diode Continuous Current	I <sub>S</sub>				225	A
<b>Dynamic Parameters</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=300KHZ		8300		pF
Output Capacitance	C <sub>oss</sub>			1510		
Reverse Transfer Capacitance	C <sub>rss</sub>			130		
<b>Switching Parameters</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =32V, I <sub>D</sub> =20A		127		nC
Gate-Source Charge	Q <sub>gs</sub>			35		
Gate-Drain Charge	Q <sub>gd</sub>			26		
Reverse Recovery Chrage	Q <sub>rr</sub>	I <sub>F</sub> =25A, di/dt=100A/us		163		ns
Reverse Recovery Time	t <sub>rr</sub>			100		
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =20V, I <sub>D</sub> =25A R <sub>GEN</sub> =2Ω		22.5		ns
Turn-on Rise Time	t <sub>r</sub>			6.7		
Turn-off Delay Time	t <sub>d(off)</sub>			80.3		
Turn-off fall Time	t <sub>f</sub>			26.9		

**Note:**

- The maximum current rating is package limited.
- Repetitive rating; pulse width limited by max. junction temperature.
- V<sub>DD</sub>=32 V, R<sub>G</sub>=25 Ω, L=0.5mH, starting T<sub>J</sub>=25 °C.
- P<sub>D</sub> is based on max. junction temperature, using junction-case thermal resistance.
- The value of R<sub>θJA</sub> is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with Ta=25 °C.

**■ Typical Performance Characteristics**

Figure.1 Typical Output Characteristics

Figure.2 Typical Gate Charge vs Gate to Source Voltage

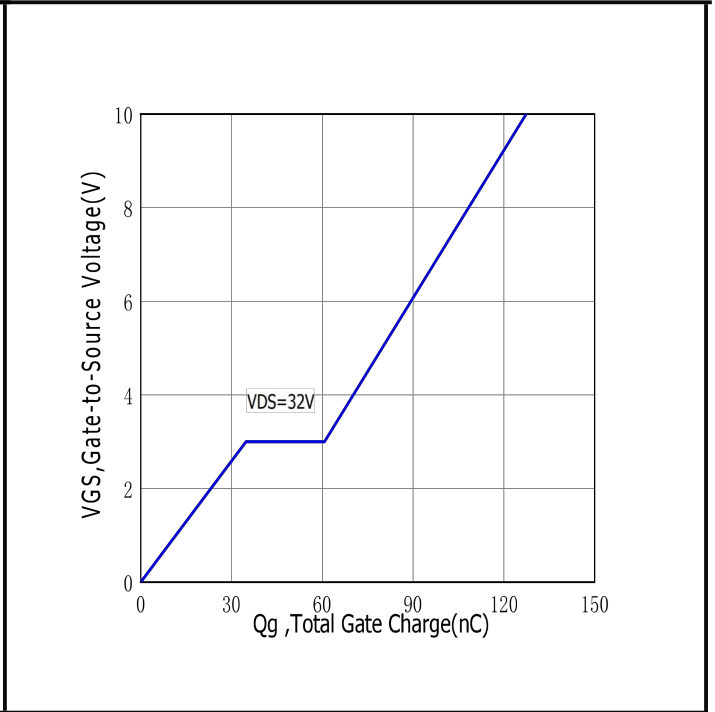
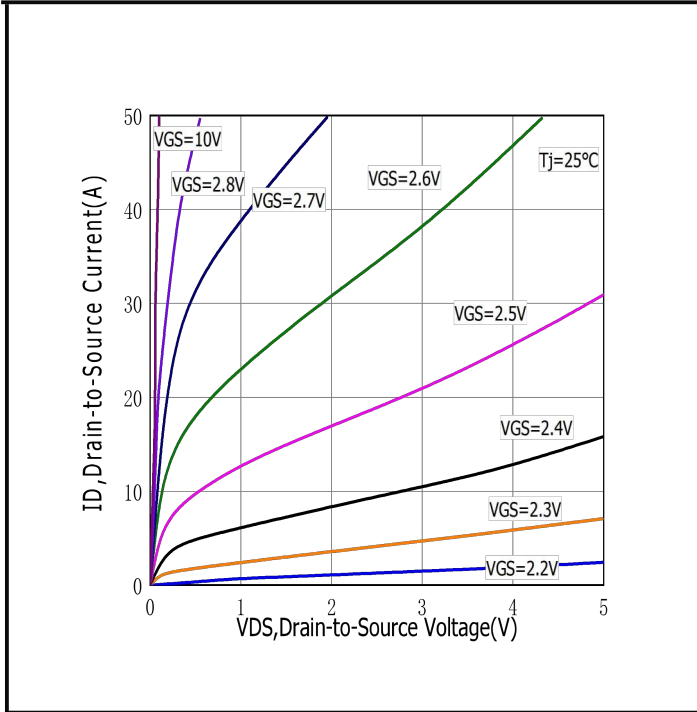


Figure.3 Typical Body Diode Transfer Characteristics

Figure.4 Typical Capacitance vs Drain to Source Voltage

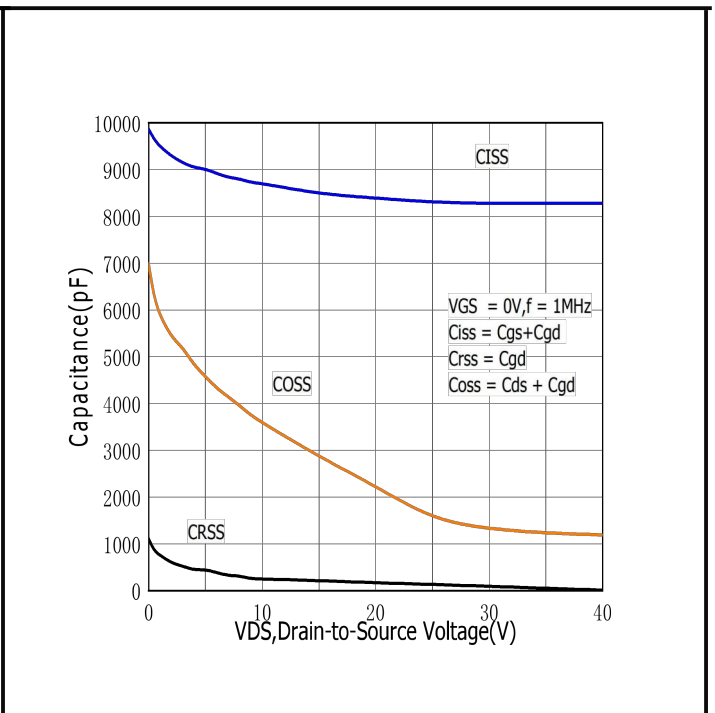
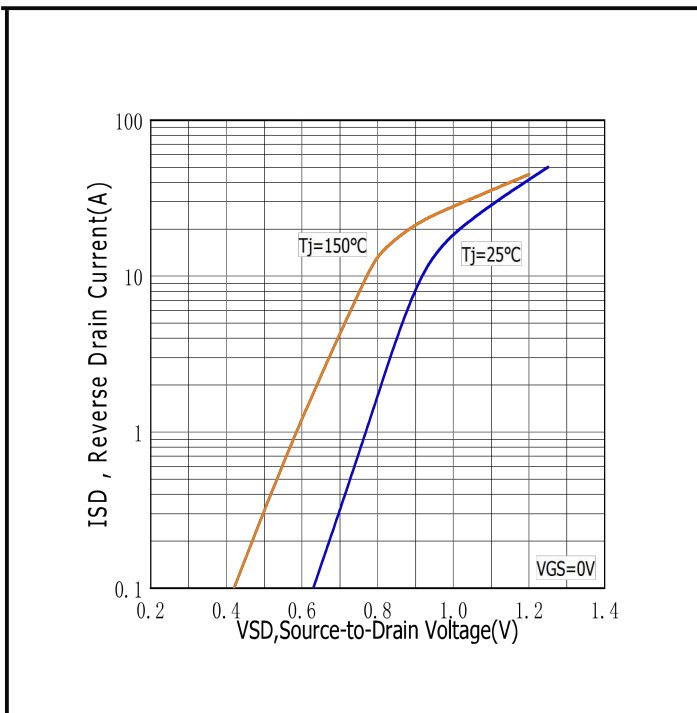


Figure.5 Typical Breakdown Voltage vs Junction Temperature

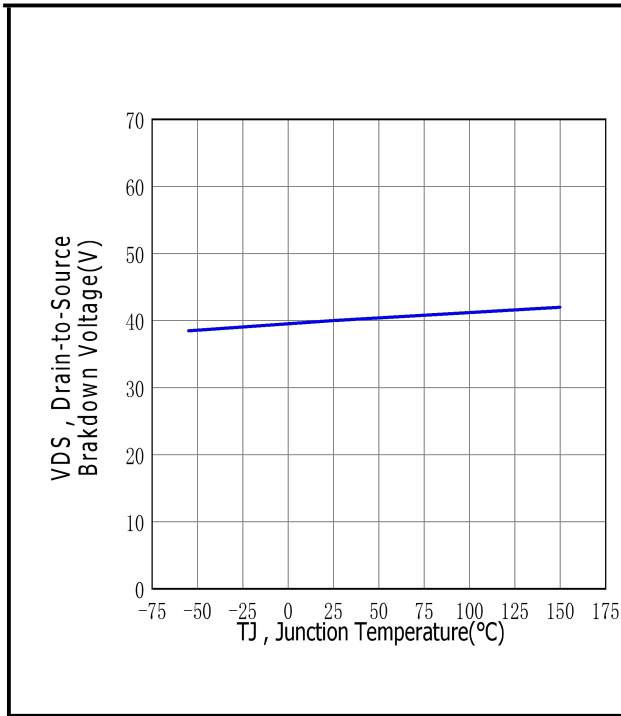


Figure.6 Typical Drain to Source on Resistance vs Junction Temperature

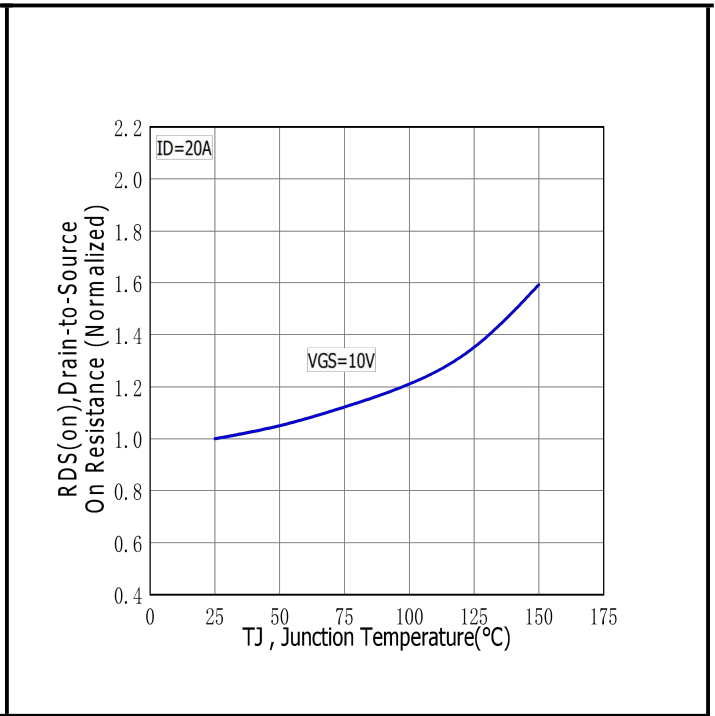


Figure.7 Maximum Forward Bias Safe Operating Area

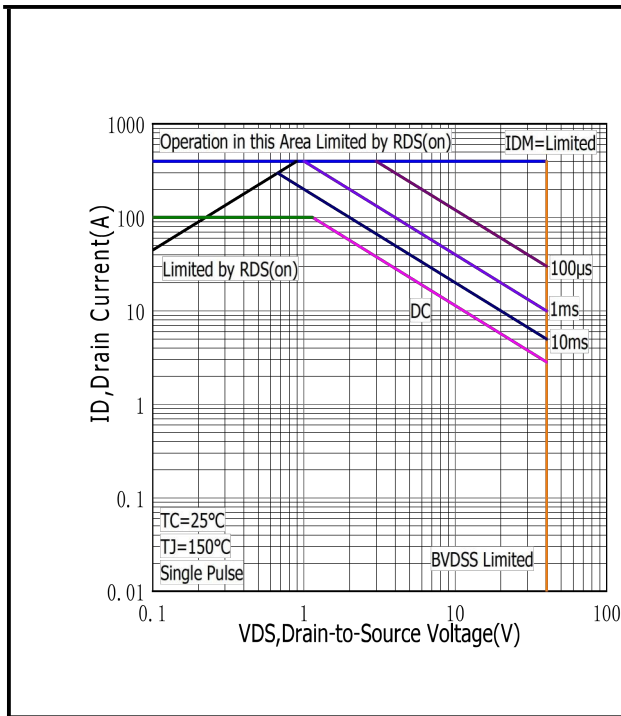
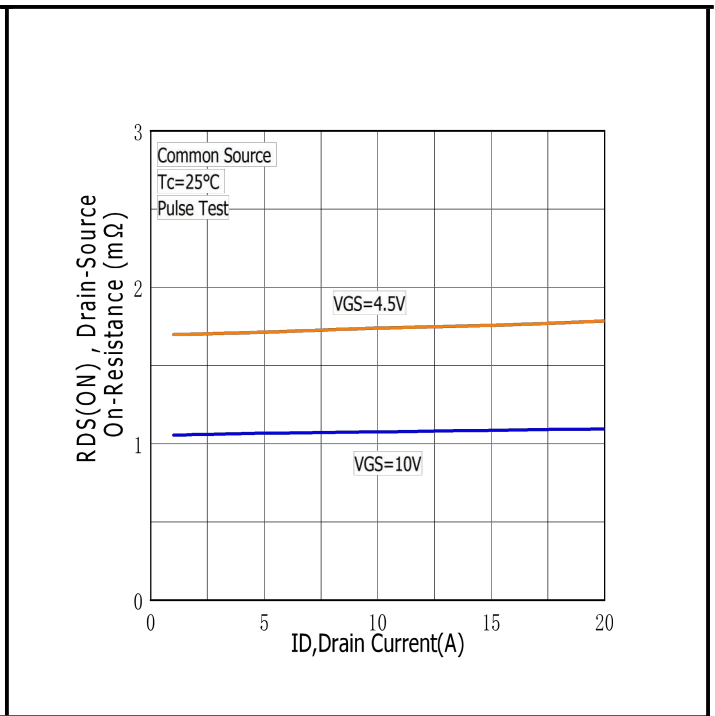


Figure.8 Typical Drain to Source ON Resistance vs Drain Current



**■ Typical Performance Characteristics**

Figure.9 Maximum EAS vs Channel Temperature

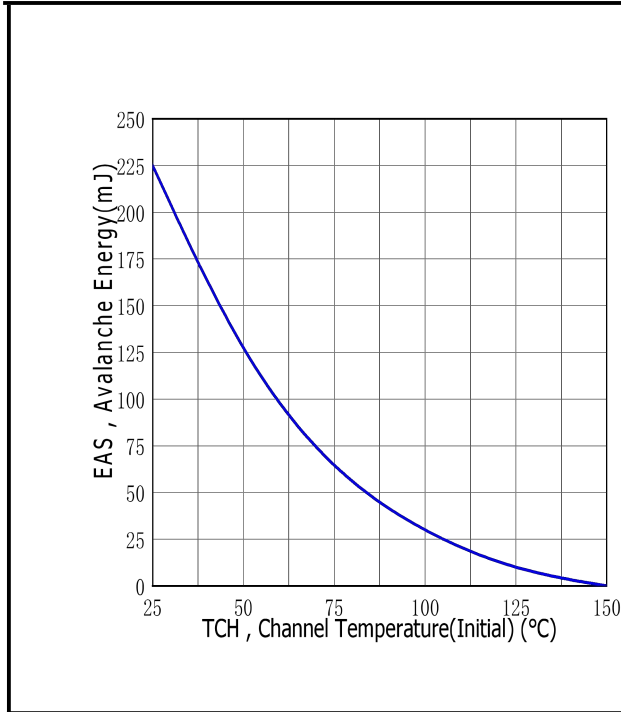


Figure.10 Typical Threshold Voltage vs Case Temperature

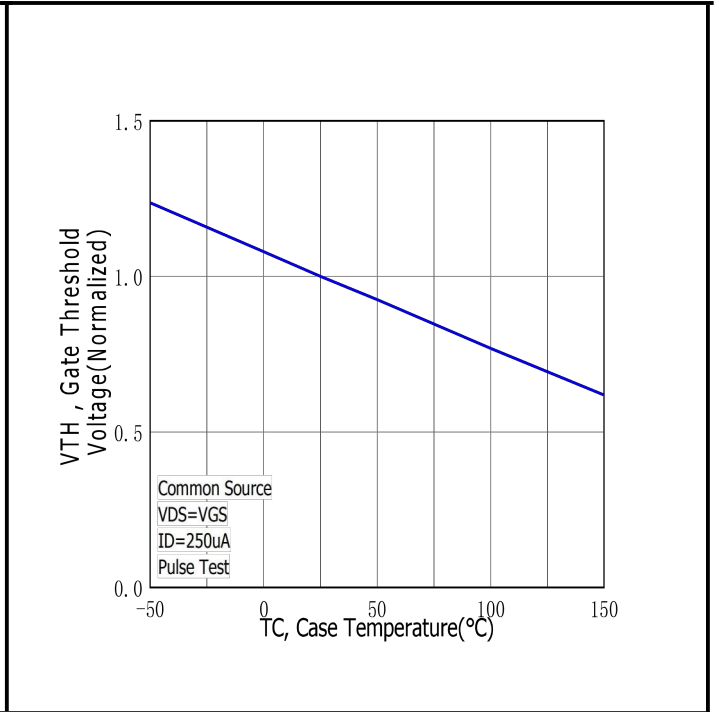


Figure.11 Typical Transfer Characteristics

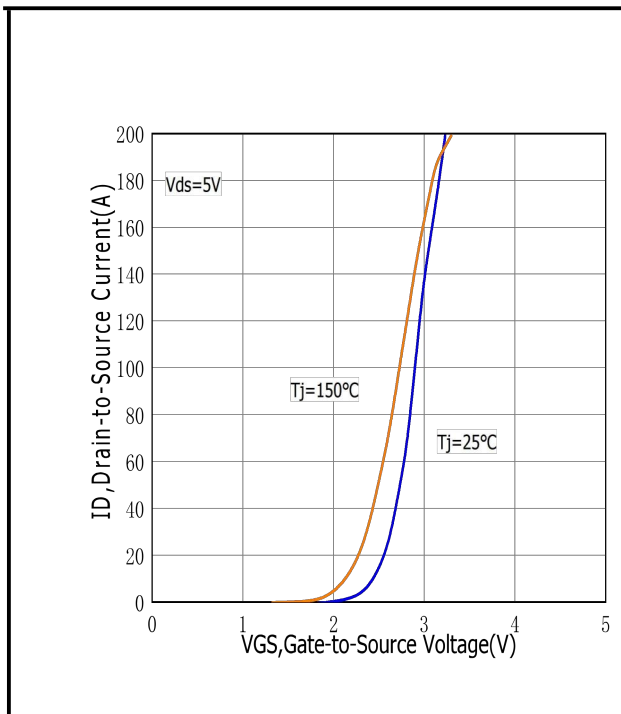


Figure.12 Maximum Power Dissipation vs Case Temperature

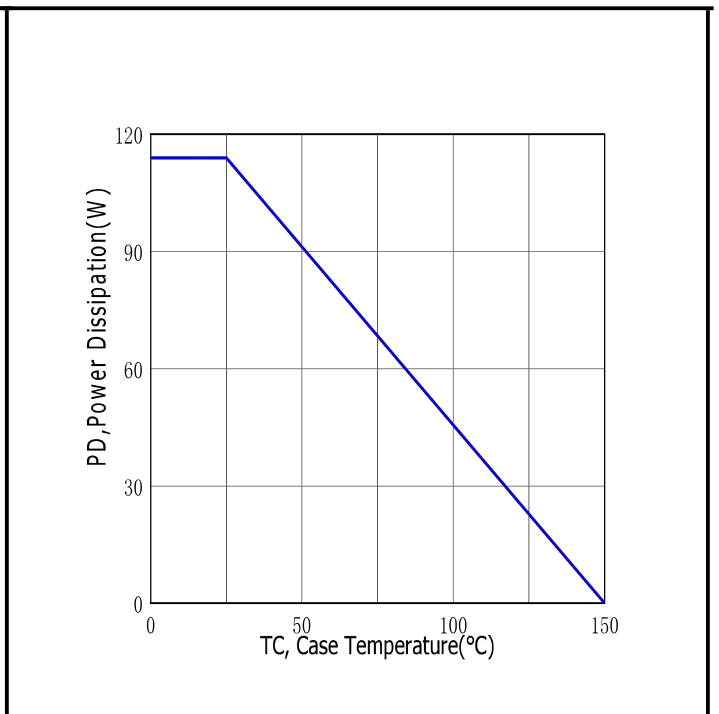
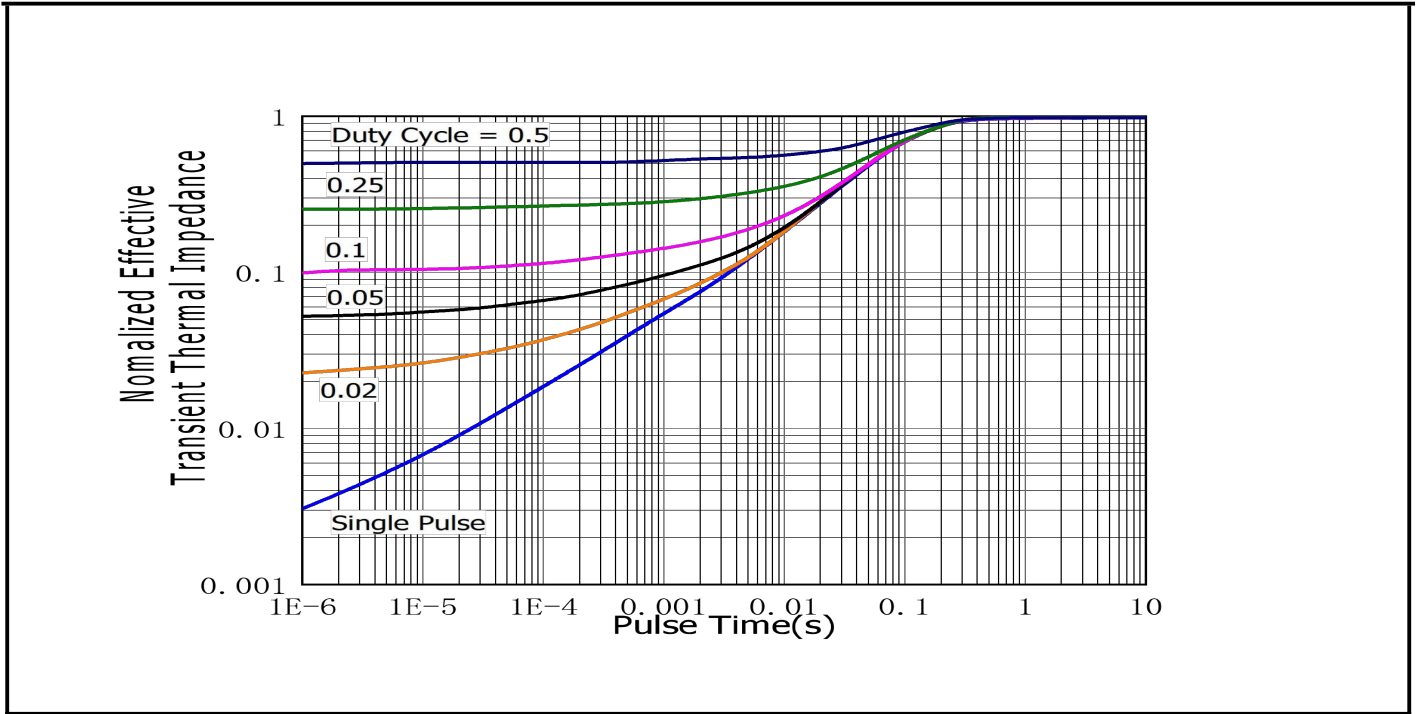


Figure.13 Maximum Effective Thermal Impedance , Junction to Case



■ Test circuits and waveforms

N-Ch 40V Fast Switching MOSFETs

Figure A: Gate Charge Test Circuit & Waveforms

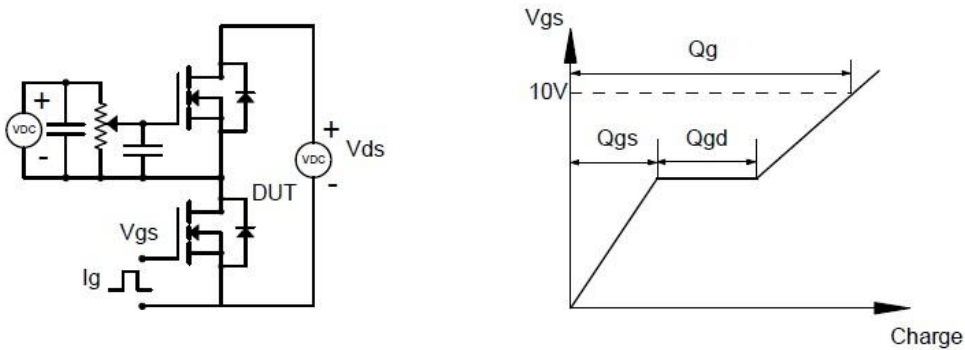


Figure B: Resistive Switching Test Circuit & Waveforms

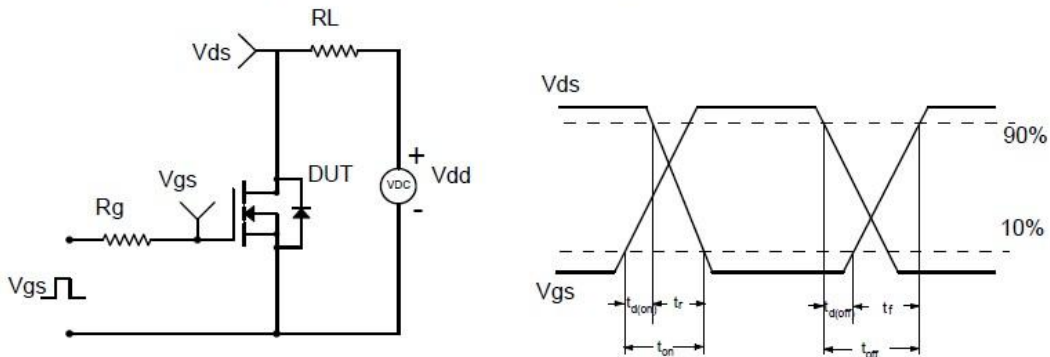


Figure C: Unclamped Inductive Switching (UIS) Test

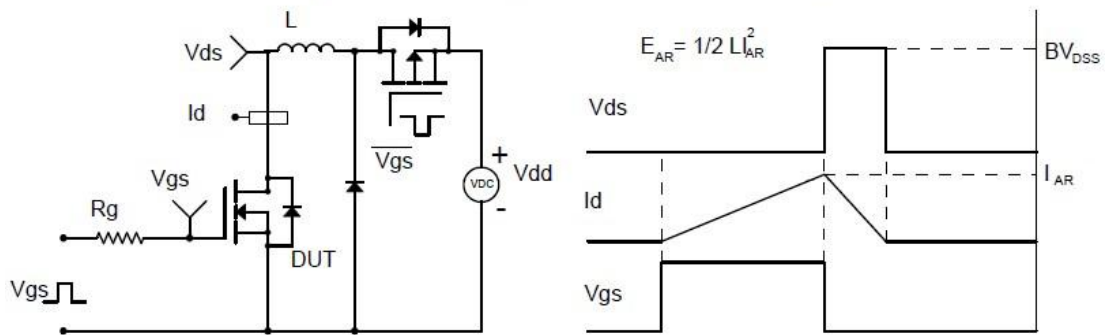
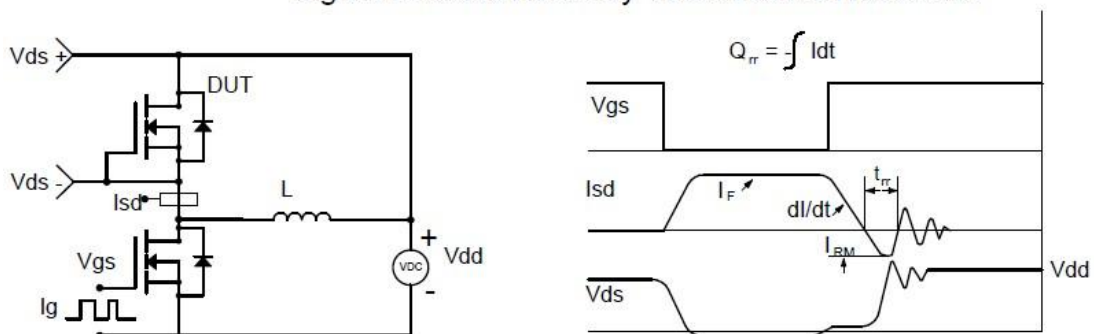
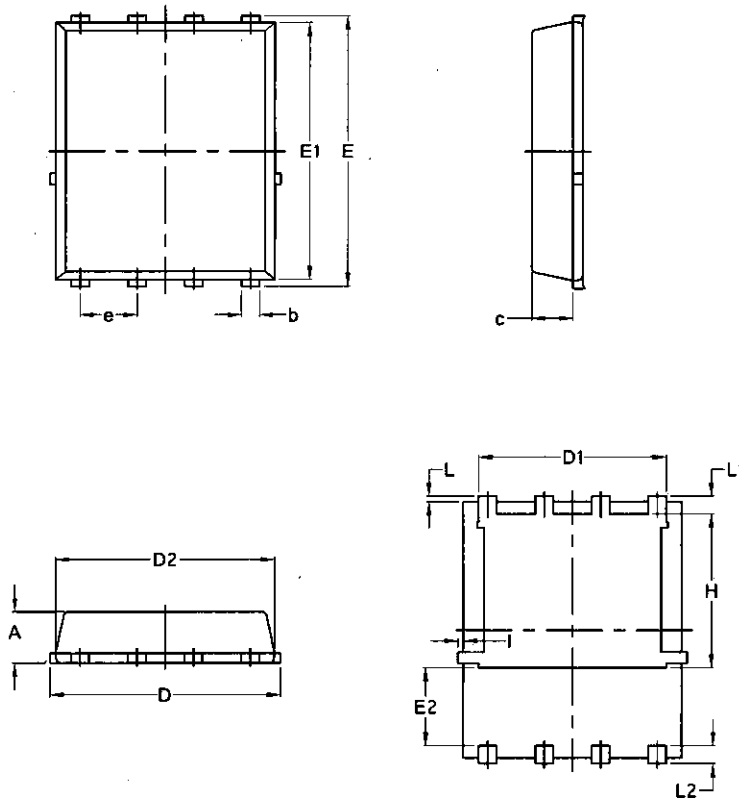


Figure D: Diode Recovery Test Circuit & Waveforms



**Package Mechanical Data-DFN5\*6-8L-JQ Single**


Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070